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Norma Slaveter
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Kazuhiko TAKADA** Group Art Unit: **2811**

Serial No.: **09/528,296** Examiner: **Ori Nadav**

Filed: **March 17, 2000** Confirmation No.: **4124**

For: **SEMICONDUCTOR DEVICE HAVING A GUARD RING**

Attorney Docket Number: **000294**
Customer Number: **38834**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

February 2, 2005

Sir:

Applicant submits herewith an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $500.00 to cover the cost for the Appeal Brief.

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If any additional fees are due in connection with this submission, please charge our Deposit Account No. 50-2866.

Respectfully submitted,

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Enclosure: Check for $500.00
Appeal Brief

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THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No: **Unassigned**

In re application of:	**Kazuhiko TAKADA**	Group Art Unit: **:2811**
Serial Number:	**09/528,296**	Examiner: **Ori Nadav**
Filed:	**March 17, 2000**	Confirmation No.: **4124**
For:	**SEMICONDUCTOR DEVICE HAVING A GUARD RING**	
Customer Number:	**38834**	Attorney Docket No.: **000294**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 2, 2005

Sir:

Applicant appeals the July 2, 2004 rejection of claims 1-4 and 7.

Applicant (now referred to hereinbelow as "appellant") filed a Notice of Appeal on December 2, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

FUJITSU LIMITED

1-1, Kamikodanaka 4-Chome

Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588

Japan

II. RELATED APPEALS AND INTERFERENCES

Appellant knows of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Pending claims 1-4 and 7 stand rejected. Claims 5 and 6 are canceled. Claims 8-12 are withdrawn from consideration. No claims are allowed or objected to. The claims on appeal are claims 1-4 and 7.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention encompasses a "semiconductor device" (*e.g.*, element 40 in Figs. 6 and 7), which includes a "substrate" (*e.g.*, element 41 in Fig. 7) and a "multilayer interconnection structure" (*e.g.*, elements 43 and 44 or elements 44 and 45 in Fig. 7) formed on the substrate.

The multilayer interconnection structure includes: "at least first and second interlayer insulation films" (*e.g.*, elements 43_1 and 43_3 in Fig. 7) provided on the substrate; and a "guard ring pattern" (*e.g.*, element 40A in Fig. 6) embedded in each of the first and second interlayer insulation films for blocking the penetration of moisture. The multilayer interconnection structure is planarized by using a chemical mechanical polishing (CMP) process. (See, *e.g.*, page 15, lines 29-31, and Fig. 8D.)

The guard ring pattern extends along a periphery of the substrate and changes its direction repeatedly and alternately in a plane parallel to the substrate. (See, *e.g.*, Fig. 6.) The guard ring pattern includes a "groove" (*e.g.*, one of elements 43_{1a}, 44_{1a}, and 45_{1a} in Fig. 7) formed in each of the first and second interlayer insulation films. The groove changes its direction repeatedly and alternatively in a plane parallel to the substrate. The guard ring pattern also includes a "conductive wall" (*e.g.*, one of elements 43_{1b}, 43_{1b}, and 45_{1b} in Fig. 7) filling the groove in each of the first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof. The guard ring pattern also includes a "conductive pattern" (*e.g.*, one of elements 43_{3b}, 44_{3b}, and 45_{3b} in Fig. 7) making contact with a top part of the conductive wall and having a principal surface coincident to the top principal surface of the interlayer insulation film. The conductive wall changes direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in the plane in correspondence to the guard ring pattern. (See, *e.g.*, Figs. 6 and 9.)

The conductive wall in the first interlayer insulation film is offset with respect to the conductive wall in the second interlayer insulation film in a direction parallel to a principal surface of the substrate when viewed in a direction perpendicular to the principal surface of the substrate. (See, *e.g.*, Fig. 7.)

The interlayer insulation films have a first insulation film (*e.g.*, element 43_1, 44_1, or 45_1 in Fig. 7) that supports the conductive wall laterally and a second insulation film (*e.g.*, element 43_3, 44_3, or 45_3 in Fig. 7) that supports the conductive pattern laterally.

In the claimed semiconductor device, the conductive wall and the conductive pattern comprise Cu. (See, *e.g.*, page 12, lines 31-33; page 13, line 36, to page 14, line 1; and page 24, lines 32-34.)

The conductive pattern and the second insulation film have coplanar top principal surfaces. A bottom edge of the conductive wall makes intimate contact with the top principal surface of the conductive pattern. (See, *e.g.*, Fig. 7.)

The conductive pattern and the second insulation film located at the top part of the multilayer interconnection structure are covered continuously with an "insulation film" (*e.g.*, element 46 in Fig. 7).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant appeals the rejection of claims 1-4 and 7 under 35 U.S.C. § 103(a) as obvious over the prior art depicted in appellant's specification, labeled "Admitted Prior Art (*APA*)," in view of *Cook et al.* (U.S. Patent No. 6,022,791) and *Chiang et al.* (U.S. Patent No. 5,817,572).

VII. ARGUMENT

Appellant presents the argument for patentability in five steps: First, appellant identifies a subset of the features of the invention that are recited in the claims. Second, appellant cites relevant MPEP requirements that are incumbent upon the Examiner for justifying his position that the invention, with the identified claim elements, would have been obvious. Third, appellant summarizes a pertinent part of how the Examiner applies prior art to show how he believes that the invention, with the identified claim elements, would have been obvious. Fourth, appellant

provides an explanation of one of the prior art references that is more in depth than that provided by the Examiner, and the resulting understanding differs significantly from that provided by the Examiner. Fifth, appellant concludes by explaining how the reference, when properly understood, cannot render the claimed invention obvious in accordance with the cited MPEP requirements.

A. The Claimed Invention

The full text of independent claim 1 is shown in the attached Claim Appendix. This claim describes a semiconductor device including a guard ring pattern, and the guard ring pattern has:

> said conductive wall *changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern* [*emphasis added*].

Claim 1 also specifies that the semiconductor device has:

> said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure being covered *continuously* with an insulation film [*emphasis added*].

Claims 2-4 and 7 depend from claim 1, so they include the cited features by virtue of their dependency.

Therefore, in accordance with the MPEP requirements discussed in the following section, to justify the obviousness rejection, the Examiner would need to assert prior art that either taught or suggested a semiconductor device that had *both*: (1) a conductive wall changing direction

repeatedly and alternately in a triangular or rectangular wave pattern; *and* (2) the top part of its multilayer interconnection structure covered continuously with an insulation film.

B. MPEP Requirements for Justifying an Obviousness Rejection

Among the requirements enumerated in the Manual of Patent Examining Procedure (MPEP) for justifying rejections, appellant cites MPEP §§ 2141 & 2143.

Under MPEP § 2143, to establish a *prima facie* case of obviousness, there must be some suggestion or motivation to modify the asserted prior art reference(s) or to combine reference teachings. Also, the prior art references when combined must teach or suggest *all* claim limitations.

Under MPEP § 2141, to combine reference teachings in support of an obviousness rejection, the prior art references must be considered *as a whole*.[1]

C. The Examiner's Justification for his Rejection

The Examiner explains his basis for the rejection in the July 2, 2004 Office Action, beginning on page 2.

The rejection relies on relies on the *APA* as the primary reference to teach a semiconductor device. More specifically, the rejection relies on conductive wall 24C (see Fig. 2 of the *APA*) to teach a "conductive wall" similar to that recited in claim 1, and the rejection also

[1] See page 2100-120, second column, to page 2100-121, first column, of the MPEP, which relies on *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

relies on protective film 26 (see again Fig. 2 of the *APA*) to teach the "insulation film" continuously covering the top of the multilayer interconnection structure as recited in claim 1.

The Examiner acknowledges that the *APA* does not teach the conductive wall changing direction repeatedly and alternately in a triangular or rectangular wave pattern as recited in claim 1. To justify the rejection, he relies instead on *Cook et al.* to suggest modifying the *APA* conductive wall (referenced sometimes in the Office Action as the "guard ring pattern") to change direction repeatedly and alternately as claimed. The Examiner writes that the modification would "reduce stress and prevent cracks" (Office Action, page 4), and he cites col. 4, lines 14-24, of *Cook et al.* (Office Action, sentence bridging pages 4 and 5).

The cited portion of *Cook et al.* discloses the following:

> However, the present inventors found that they could provide a crack stop that was nearly as efficient as a traditional air fill-type crack stop without adding any additional masking or etching steps simply by providing a crack stop ring in a geometric pattern, such as serpentine ring 60. The serpentine pattern sufficiently increases both the area of the crack stop and the stress relaxed volume surrounding the crack stop so that fracture resistance is substantially increased and fracture driving force is substantially decreased, as shown by the data in Table 1 below.

Although in isolation, that is, without considering the reference *as a whole*, this excerpt might seem to support the Examiner's rejection, appellant explains in the next section why a proper understanding of the reference renders it inadequate as a motivation to modify the *APA* semiconductor device to have all of the features recited in the claims.

D. The *Cook et al.* Crack Stop

Cook et al. describes structures for preventing cracks from propagating from the edges of a semiconductor chips into the chip active area. Dicing semiconductor wafers was known to cause such cracks. (Col. 1, lines 4-16.) *Cook et al.* discusses one type of crack stop in the paragraph beginning in col. 3 at line 48, and in the next paragraph, beginning in col. 4 at line 1, *Cook et al.* discusses a variation of the first type of crack stop.

The first type of crack stop, ring 50[2] (Figs. 4a and 4b), does not change direction repeatedly and alternately in a triangular or rectangular wave pattern as claimed. Instead, ring 50 is straight, so it is analogous to the *APA* guard ring structure 12 (Fig. 1B). Unlike the *APA* guard ring structure 12, however, the conductor in the *Cook et al.* ring 50 is etched out. Thus, ring 50 is "empty," and the disclosure calls this type of crack stop an "air fill type crack stop" (col. 3, lines 52-53).

It is important to recognize that a semiconductor device having an air fill type crack stop *cannot* have an "insulation film" continuously covering the top part of its multilayer interconnection structure as described in appellant's claim 1. Although Fig. 4b shows some metal remaining in ring 50, the figure also clearly shows a gap in the top passivation films.

As noted above, the Examiner relies on the *Cook et al.* discussion of the second type of crack stop, and this type changes direction repeatedly and alternately in a triangular or rectangular wave pattern analogously to the conductive wall described in claim 1. The *Cook et*

[2] The disclosure labels this element "straight *fine* crack stop ring 50" (col. 3, lines 48-49). In the context of the disclosure as a whole, it seems that the term "straight *line* crack stop ring 50" may have been intended, and the label provided could be a typographical error.

al. inventors developed this type of crack stop to reduce the costs involved in removing multiple layers of metal from the crack stop ring. (Col. 3, lines 57-67.)

However, it is also important to realize that *Cook et al.* does *not* teach that the second type of crack stop will have no air fill crack stop at all. As clearly shown in Figs. 4b, 5c, 6b, and 7c, the *Cook et al.* crack stops include air-filled trenches in the top passivation films. (Please note the attached annotated cover page of the *Cook et al.* patent document, in which the air fill crack stop of the Fig. 6b embodiment is labeled.) Consequently, even with the second type of crack stop, there can be no "insulation film" continuously covering the top part of the semiconductor device's multilayer interconnection structure as described in appellant's claim 1.

Appellant respectfully submits to the Board his conclusion that, if *Cook et al.* had intended to teach that the second type of crack stop would have no air-filled region at all, Figs. 4b, 5c, 6b, and 7c would not show the discontinuities in the upper passivation films above the crack stop rings. Appellant submits that *Cook et al.* teaches one skilled in the art that the second type of crack stop has an air-filled region in the upper passivation films and a conductive ring below that changes direction repeatedly and alternately.

E. The Limitations Preventing *Cook et al.* from Suggesting a Modification of the *APA* Semiconductor Device to Obtain the Claimed Invention

Cook et al. cannot suggest modifying the *APA* semiconductor device to obtain the claimed invention. Appellant discusses here two ways of applying the *Cook et al.* teachings summarized above, and appellant explains why neither application would conform to the MPEP

requirements cited above. The first way discussed below is to rely on the *Cook et al.* teaching of a crack stop having both: (1) an air-filled region in the upper passivation films; and (2) a conductive ring below that changes direction repeatedly and alternately. The second way of applying the *Cook et al.* teachings is to selectively rely on the *Cook et al.* teaching of a conductive ring changing direction repeatedly and alternately while disregarding the accompanying teaching of an air-filled region in the upper passivation films. The Examiner applies the *Cook et al.* teachings in the second way.

1. **Applying the *Cook et al.* teaching of a crack stop, which has both: (1) an air-filled region in the upper passivation films; and (2) a conductive ring below that changes direction repeatedly and alternately, yields a semiconductor device without the claimed "insulation film" continuously covering the top part of the semiconductor device's multilayer interconnection structure.**

As discussed in the previous section, *Cook et al.* teaches a crack stop has both: (1) an air-filled region in the upper passivation films of the semiconductor device; and (2) a conductive ring below the air-filled region that changes direction repeatedly and alternately. If the *APA* semiconductor (Figs. 1A, 1B, and 2) device were modified to have a crack stop with both of these features, the *APA* protective film 26 would no longer continuously cover the multilayer interconnection structure as described in the claims. Under MPEP § 2143, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest *all* claim limitations. Therefore, because the combination of *APA* and *Cook et al.* do not yield a semiconductor device with the continuous cover of an insulation film as claimed, the

combination does not conform to MPEP § 2143 and therefore cannot support an obviousness rejection.

2. Selectively applying the *Cook et al.* teaching of a conductive ring changing direction repeatedly and alternately, while disregarding the accompanying teaching of an air-filled region in the upper passivation films, does not comply with the MPEP requirement to consider a prior art reference as a whole.

The Examiner relies on the *Cook et al.* teaching of a conductive ring changing direction repeatedly and alternately, but he disregards the accompanying teaching of an air-filled region in the upper passivation films. That is, the Examiner does not consider the *Cook et al.* reference *as a whole* as required by MPEP § 2141.

The Examiner does not provide any reason why it supposedly is not necessary to apply the teaching of the upper air-filled region when he applies the accompanying teaching of the conductive ring changing direction repeatedly and alternately. As appellant describes above, the two teachings are presented by *Cook et al.* together as the way to form the crack stop. The Examiner provides no explanation of why *Cook et al.* would teach the extra requirement of adding an upper air-filled region to its semiconductor device if it were not needed as part of the crack stop.

Therefore, because the Examiner does not consider the *Cook et al.* reference *as a whole*, the rejection should be reversed.

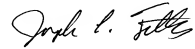
In view of the reasons provided above, appellant solicits the reversal of the obviousness rejection of claims 1-4 and 7 under 35 U.S.C. § 103(a).

VIII. CONCLUSION

For the above reasons, appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's rejection of claims 1-4 and 7.

In the event this paper is not timely filed, appellant petitions for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 50-2866, along with any other additional fees that may be required with respect to this paper.

Respectfully submitted,
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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Enclosures: Claims appendix
Evidence appendix
Related proceedings Appendix
Annotated cover page of *Cook et al.* patent

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CLAIMS APPENDIX

The following claims are involved in the present appeal:

Claim 1: A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films for blocking penetration of moisture, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate,

and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally,

said conductive wall and conductive pattern comprising Cu,

said conductive pattern and said second insulation film having coplanar top principal surfaces,

a bottom edge of said conductive wall making an intimate contact with said top principal surface of said conductive pattern, and

said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure being covered continuously with an insulation film.

Claim 2: A semiconductor device as claimed in claim 1, wherein said guard ring pattern extends continuously along said periphery of said substrate.

Claim 3: A semiconductor device as claimed in claim 1, wherein said conductive pattern extends in the form of a straight line along a peripheral edge of said substrate.

Claim 4: A semiconductor device as claimed in claim 1, wherein said conductive pattern changes a direction thereof repeatedly and alternately in said plane in correspondence to said conductive wall.

Claim 7: A semiconductor device as claimed in claim 1, further comprising an etching stopper layer interposed between said first insulation film and said second insulation film.

EVIDENCE APPENDIX

No evidence under 37 C.F.R. § 41.37(c)(1)(ix) is submitted.

RELATED PROCEEDING APPENDIX

No decisions under 37 C.F.R. § 41.37(c)(1)(x) are rendered.

ANNOTATED COVER PAGE OF *Cook et al.* PATENT

US006022791A

United States Patent [19]

Cook et al.

[11] **Patent Number: 6,022,791**

[45] **Date of Patent: Feb. 8, 2000**

[54] **CHIP CRACK STOP**

[75] Inventors: **Robert Francis Cook**, Putnam Valley, N.Y.; **Eric Gerhard Liniger**, Danbury, Conn.; **Ronald Lee Mendelson**, Richmond; **Richard Charles Whiteside**, Charlotte, both of Vt.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **08/950,691**

[22] Filed: **Oct. 15, 1997**

[51] **Int. Cl.**[7] **H01L 21/30**; H01L 21/46

[52] **U.S. Cl.** **438/458**; 438/460; 438/462; 438/928

[58] **Field of Search** 438/458, 460, 438/462, 928; 257/508, 620

[56] **References Cited**

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Primary Examiner—John F. Niebling
Assistant Examiner—David A. Zarneke
Attorney, Agent, or Firm—James M. Leas

[57] **ABSTRACT**

A serpentine pattern has been found to be effective at interrupting propagation of delamination cracks in thin film layers. The ring is provided on a semiconductor chip to suppress crack propagation from the chip edge. The ring is effective even though it is filled with metal, the serpentine pattern providing significantly increased area as compared with a standard linear crack stop that the energy for crack propagation is dissipated. In addition to serpentines, pattern features such as staggered filled ring patterns and connected rings will also be effective at reducing the propagation of delamination cracks from edge to active area by virtue of the increased area of interaction between the crack and the crack stop.

15 Claims, 11 Drawing Sheets